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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/820,049	03/28/2001	Carl K. Abrahamson	TA 014	3090

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EXAMINER	
CRAIG, DWIN M	

ART UNIT	PAPER NUMBER
2123	

DATE MAILED: 08/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/820,049	ABRAHAMSON, CARL K.	
	Examiner	Art Unit	
	Dwin M. Craig	2123	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2 and 4-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 2 and 4-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 2 and 4-12 are presented for reconsideration based on Applicant's arguments, amended claim language and Request for Continued Examination (RCE) under 37 CFR 1.114.

2. Dwin Craig is the current Examiner of record. Eduardo Otero-Garcia is no longer the Examiner of record.

Response to Arguments

3. Applicant's arguments submitted in the 14 June 2005 reply have been fully considered. The Examiner's response is as follows;

3.1 As regards the Applicant's response to the 35 USC § 112 rejections of the claims.

The Examiner has found Applicant's arguments to be persuasive and withdraws the 35 USC § 112 rejections of the claims. The Examiner thanks the Applicant for amending the preamble of claim 1.

3.2 As regards the Applicant's response to the 35 USC § 103 rejections of claims 1, 2, 4-12 the Examiner has found the argument of page 6 of the 14 June 2005 response to be persuasive and withdraws the earlier art rejections of the claims.

3.3 An updated search has revealed new art.

Drawings

4. The Examiner objects to the drawings under 37 CFR 1.83, the Examiner requires that the different boxes in Figures 1 and 2 be labeled, for example in figure 1 item 38 should be labeled "configurable electronic circuit" and item 40 should be labeled "configuration control element", further, and as another example, the box with item 46 should be labeled "In-System Programmer". The Examiner observes that the current drawings only contain item numbers and

do not faithfully render the claimed configuration of Applicant's invention in a manner that is essential for a proper understanding of the invention.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1, 2, 4-7 and 11 are rejected under 35 USC § 102(e) as being anticipated by US Patent 6,052,773 DeHon et al.

5.1 As regards independent claims 1 the *DeHon et al.* reference discloses,

An electronic component electronically connected with an external electronic master system comprising:

configurable electronic circuitry means for emulating an output signal from a respective known electronic system sub-component of a known electronic master system, the output signal corresponding to a function of the electronic system sub-component; (Figure 1 item 10 is the Master system, Figure 3B Item A and Item 100c the Reconfigurable I/O unit is the sub-system component),

an input/output interface for electronically mating the configurable electronic circuit means to the electronic master system; (Figure 1 item 12 "CONFIG. INTERF.),

a configuration controller element electronically connectable with the configurable electronic circuit means, the configuration controller determines the location of the configurable electronic circuitry means in the electronic master system and configures the configurable electronic circuitry means to emulate a selected function and operational characteristics of the known electronic system sub-component; and (Col. 22 line 54, "Thus, any 4 input x1 output logic operation is emulated." and Figure 7A),

the configurable electronic circuitry means has an output adaptable as an input to the electronic master system to replicate and replace functions of the known electronic system sub-component acting in the electronic master system. (Figure 1 item 11 DATA and item 13 DATA and Figures 3A, 3B and 3C which disclose reconfigurable I/O units that can be used to replace functions of a known electronic subsystem like a UART, for example.).

5.2 As regards dependent claims 2 and 9 the *DeHon et al.* reference discloses (Col. 3 line 4 "In specific implementations, the configurable interface is connected to address and data lines of on-chip buses of the processor and input/output pads for off-chip communications." The Examiner notes that "off-chip communications" infers that there is a circuit card assembly or circuit board). The Examiner further notes that the explanation of interfacing the processor as disclosed involves *"interfacing with a system"* which infers the use of a circuit board, *see* (Col. 18 line 55-63).

5.3 As regards dependent claim 4 the *DeHon et al.* reference discloses a processor means (Figure 1 item 10 "FIXED PROCESSOR CORE CELL").

5.4 As regards dependent claim 5 the *DeHon et al.* reference discloses a memory means (Figure 2F item 570, for example, the Examiner notes that there are other disclosures of memory means in the *DeHon et al.* reference and is only discussing the one example in Figure 2F).

5.5 As regards dependent claim 6 the *DeHon et al.* reference discloses digital logic circuitry (All of the figures teach digital logic and Col. 3 lines 32-38).

5.6 As regards dependent claim 7 the *DeHon et al.* reference discloses emulation (Col. 22 line 54, "Thus, any 4 input x1 output logic operation is emulated." and Figure 7A).

5.7 As regards dependent claims 11 the *DeHon et al.* reference discloses an FPGA (Col. 21 lines 17-20).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

6. Claims 8, 9, 10 and 12 are rejected under 35 USC § 103(a) as being unpatentable over US Patent 5,717,903 Bonola in view of US Patent 6,438,737 Morelli et al.

6.1 As regards independent claim 8 the *Bonola et al.* reference discloses;

"electronic circuitry means for emulating an output signal; from a respective known electronic system sub-component of a known electronic master system, the output signal corresponding to a function of the electronic system sub-component" (Abstract, Col. 6 lines 24-51).

"an input/output interface for electronically mating the electronic circuitry means to the electronic master system" (Figure 1 item 24, *for example*).

" a configuration controller element electronically connectable with the electronic circuitry means the controller determines the location of the electronic circuitry means in the electronic master system and configures the electronic circuitry means to emulate a selected function and operational characteristics of the known electronic system sub-component" (Abstract, Col. 6 lines 24-51).

"the electronic circuitry means has an output adaptable as an input to the electronic master system to replicate and replace functions of the known electronic system sub-component acting in the electronic master system." (Col. 3 lines 47-56, further, it is noted by the Examiner that the *Bonola et al.* reference discloses the teaching of a CPU based system for emulating a computer peripheral, which in and of itself describes a system and a method of providing the emulation of a system sub-component with input and output signals, further, the Bonola reference discloses that the CPU's on each adapter card can be re-programmed to emulate different subsystem components *i.e. computer peripherals.* As regards the use of a "*Master System*" see Col. 2 lines 12-15).

However, the *Bonola* reference does not expressly disclose the use of configurable logic or FPGA's for circuit emulation.

The *Morelli et al.* reference discloses the use of configurable logic circuits for use in emulation systems (Abstract, Figure 1 item 40, Col. 4 Lines 12-38, *for example*).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used configurable logic circuits in the design of an emulation system because of the flexibility and decreased development time the addition of FPGA's or PLD's provide to any digital design that is being contemplated. Further, the advantage that FPGA or PLD design methods provide by allowing hardware implementations to be tested without the need for actually fabricating an ASIC, provide for a savings in cost over the previous methods of testing hardware designs. It is also noted by the Examiner that the *Morelli et al.* reference discloses that (Col. 1 lines 12-19, "Programmable Logic Devices (PLDs) have been developed to facilitate testing and modification of a digital logic design *before* committing it to mass production. Because these devices fill a unique gap between software data processing and dedicated hardware data processing, some have attempted to augment existing computer systems by installing an input/output (I/O) module with a software accessible programmable logic device"), it is noted by the Examiner that this last section of the *Morelli et al.* reference, *specifically* addresses the expressly claimed limitation of, *"an input/output interface for electronically mating the electronic circuitry means to the electronic master system"*. Therefore, the Examiner notes that due to the technical advantages, expressly disclosed by the *Morelli et al.* reference as cited in this Office Action, that objective evidence has been presented to demonstrate that an artisan of ordinary skill, *without any knowledge of Applicant's claimed invention,* would have used the methods set forth in the *Morelli et al.* reference in combination with the emulation methods set forth in the *Bonola* reference.

6.2 As regards dependent claim 9 the *Bonola et al.* reference discloses a circuit board connected to a Master System (Figure 1 items 20, 21, 22, and 23 for example...).

6.3 As regards dependent claim 10 the *Bonola et al.* reference discloses, a removable circuit board (Figure 1 items 20, 21, 22, and 23 for example...Col. 3 lines 10-24).

6.4 As regards dependent claim 12, the *Bonola et al.* reference does not expressly disclose the use of FPGA's.

The *Morelli et al.* reference discloses the use of configurable logic circuits for use in emulation systems (Abstract, Figure 1 item 40, Col. 4 Lines 12-38, *for example*).

It would have been obvious, to one of ordinary skill in the art, at the time the invention was made, to have used configurable logic circuits in the design of an emulation system because of the flexibility due to an FPGA being re-programmable provides to any design that is being contemplated and specifically for method of emulation of logic designs as claimed by the Applicant.

Conclusion

7. **Claims 1, 2 and 4-12** have been presented for reconsideration based on Applicant's amended claim language, arguments and Request for Continued Examination (RCE). Claims 1, 2 and 4-12 have been rejected. The drawings have been objected to.

7.1 Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dwin M. Craig whose telephone number is (571) 272-3710. The examiner can normally be reached on 10:00 - 6:00 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo P. Picard can be reached on (571) 272-3749. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DMC

Paul L. Rodriguez 8/22/05
Primary Examiner
Art Unit 2125